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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/172,298
Filing Date: October 14, 1998
Appellant(s): RHODES, HOWARD E.

Mark J. Thronson
Megan S. Woodworth
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 13, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The Brief is deficient because the Brief (page 3) does not explain limitations of independent claims 14, 28, 39 and 53. Claim 14 (Figure 1, pages 5-7) has a "readout circuit" comprising "output transistor" 36 for "reading out charge from a node" 30, and "reset transistor" 32. Claims 28 and 39 also have a "reset device" 32 to "periodically reset the voltage of said diffusion node" 30. Claims 28 and 39 (Figures 1, 2; pages 5-12) have a "plurality of active pixel sensors" 200 (page 5, lines 16-25; page 9, line 29 et seq), a "row decoder" 220, and a "plurality of output circuits" 60. Claim 53 (Figure 1) has a "processor" 60.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

4,143,389	Koike	3-1979
4,385,307	Suzuki	5-1983
5,241,198	Okada	8-1993
5,307,169	Nagasaki	4-1994
5,804,845	Anagnostopoulos	9-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The process terminology (claims 31, 32, 38, 41, 42, 51, etc) is considered only in terms of a *necessary resultant* structure from the process. The process itself is not at issue. The device claims are *not* limited to the recited process. See MPEP 2113; *In re Brown*, 173 USPQ 685 (CCPA 1972); *In re Fitzgerald*, 205 USPQ 594 (CCPQ 1980); *In re Marosi*, 218 USPQ 289, 292, 293 (CCPA 1983); *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985). In terms of resultant structure, a "grown layer" or "deposited layer" is taken as a layer.

Claims 1-4, 7-13 and 120 stand rejected under 35 USC 102 as unpatentable as shown by Anagnostopoulos et al. See Figures 2A, 3A, 3B, 3C, with a "photosensitive area" 11 or 12 within the "substrate" 26, 24. The "nitrogen containing second insulating" layer reads on an ONO (oxide-nitride-oxide) layer or NO (nitride-oxide) layer as in Anagnostopoulos et al. See present claims 9-13, which encompass an ONO layer or NO layer as the "nitrogen containing second insulating" layer, where then an oxide layer is "in contact with said substrate," since an ONO layer has three sublayers: silicon oxide on silicon nitride on silicon oxide, and a NO layer has two sublayers: silicon nitride on silicon oxide.

For claim 4, in Figure 3A, the "first" & "second" gate stacks read on electrodes 32 with indium tin oxide "photogate" 30. The "nitrogen containing second insulating layer" reads on an ONO layer 35, 34, 36 "in contact with said substrate and beneath said photogate" 30 (claims 8, 9), that is spatially "distinct from said first insulating" layer, which reads on silicon oxide layer 36 beneath electrodes 32 (claim 120). An ONO layer comprises a "silicon nitride" layer (claim 7), a "NO" layer (claims 8, 10) and an "ON" layer (claim 11). In Figures 3B and 3C, the

"nitrogen containing second insulating" layer reads on an ONO layer 41, 42, 43 (Figure 3B) (claims 8, 9) or NO layer 51, 52 (Figure 3C) (claim 10) "in contact with said substrate" and "beneath said photogate" 30 that is spatially "distinct from said first insulating" layer, which reads on silicon oxide layer 43 (Figure 3B), and layer 52 (Figure 3C) "beneath" electrodes 32 (claim 120).

For claim 2, as an alternative in Figures 3B, 3C, the "first" & "second" gate stacks read on electrode 30 with polysilicon "photogate" 32. The "nitrogen containing second insulating" layer reads on an ONO layer 41, 42, 43 (Figure 3B) (claim 13) or NO layer 51, 52 (Figure 3C) "in contact with said substrate" and "beneath said photogate" 32 that is spatially "distinct from said first insulating" layer, which reads on silicon oxide layer 43 (Figure 3B) and layer 52 (Figure 3C) "beneath" electrode 30. An ONO (oxide-nitride-oxide) layer comprises a "silicon nitride" layer (claim 12).

Claims 1, 3, 7, 14, 15, 18, 19, 26, 28, 29, 31-33, 38, 39, 41, 42, 44, 46, 51, 53, 55, 57-59, 115-125 and 135-139 stand rejected under 35 USC 103 as unpatentable over the acknowledged prior art in this application (Figures 1, 2, pages 1-12) and Nagasaki et al, considered together. For an imaging device as in the acknowledged prior art (Figures 1, 2), it would have been obvious to use an insulator with higher dielectric constant "beneath" photogate 24 as suggested by Nagasaki et al (Figures 3, 6, 17; columns 2-3), in order to increase the capacity of the photogate. From Nagasaki et al (column 2 lines 22-24, column 3, table 1), both silicon nitride and silicon oxide were conventional materials for use as a photogate insulator, which would have been obvious to use as a photogate insulator. From Nagasaki et al, it would have been obvious that the materials used in this invention, e.g., conventional silicon nitride as in claims 7, 19, 33, 46 and 59, would achieve a higher capacity of the photogate than use of

conventional silicon oxide. Thus, it would have been obvious to use conventional silicon nitride, as in claims 7, 19, 33, 38, 46, 51, 59 and 115-119, in order to achieve a higher capacity of the photogate than the use of conventional silicon oxide. From Nagasaki et al (column 3,table 1), it also would have been obvious that the materials used in this invention would achieve a lower capacity of the photogate than would use of tantalum oxide, because tantalum oxide has a higher dielectric constant than silicon nitride, while silicon nitride has a higher dielectric constant than silicon oxide.

The acknowledged prior art (Figures 1, 2) shows claimed elements. The "transparent or semi-transparent" photogate (claims 3, 26, 44, 55) reads on photogate 24. The "node" (claims 14, 28, 39) reads on floating diffusion region 30. The "readout circuit comprising at least one output transistor" (claim 14) reads on source follower transistor 36. The "second gate stack" (claims 1, 135), "reset" transistor (claim 14) and "reset" device (claims 28, 39) read on reset transistor 31 with gate 32. The "plurality of active pixel sensors" (claims 28, 39) read on pixel array 200. The "row decoder" (claims 28, 39) reads on row decoder 220. An "output" circuit (claims 28, 39) and "processor" (claim 53) read on a readout circuit 60. The "first gate stack" (claims 1, 135), "charge transfer" device (claims 15, 18), "transfer transistor" (claim 29), and "transfer transistor gate stack" (claims 121-124, 139) read on transfer transistor 29 with gate 28. The "layer of silicon dioxide" (claims 120-125) reads on silicon diode layer 22 that is beneath gate 28 and gate 32.

In Nagasaki et al (Figures 3, 6), transparent electrode 21 corresponds to photogate 24 of acknowledged prior art Figure 1. Regions 2, 3 and gate electrode 6 (Figures 3, 6) correspond to regions 26, 30 and gate 28. In Figure 6, silicon dioxide is used beneath gate electrode 6, just as silicon dioxide is used beneath gate 28 in acknowledged prior art Figure 1.

The conclusion is that the claimed invention as a whole would have been obvious at the time the invention was made. The hypothetical person of ordinary skill in the relevant art, familiar with all that the acknowledged prior art and Nagasaki et al disclose, "would have found it obvious to make a structure corresponding to *what is claimed.*" *In re Sovish*, 226 USPQ 771, 774 (Fed. Cir. 1985).

Claims 2, 4, 25, 27, 43, 45, 54, 56, 126-134 and 140-144 stand rejected under 35 USC 103 as unpatentable, the evidence being the acknowledged prior art in this application (Figures 1, 2, pages 1-12) and Nagasaki et al, applied as in the above rejection, further considered together with Koike et al. The claimed materials (claims 2, 4, 25, 27, 43, 45, 54, 56) are conventional to use as transparent or semi-transparent materials, as applicant would agree and as shown by Koike et al (columns 3-4), which would have been obvious to use to achieve a transparent or semi-transparent photogate electrode. Note that "tin oxide" reads on SnO_2, "indium oxide" reads on InO_2 and "polysilicon" is polycrystalline silicon. Moreover, it would have been obvious to have the photogate insulator extend over an adjacent "gate stack" (claims 126-134, 140-144) as the photogate insulator does over gate stack 18 of Koike et al (Figure 2), in order to achieve a photogate insulator and adjacent gate 28 as in the acknowledged prior art in this application (Figure 1).

In Koike et al (Figure 2), transparent or semi-transparent electrode 22 corresponds to transparent electrode 21 of Nagasaki et al (Figures 3, 6) and photogate 24 of acknowledged prior art Figure 1. Regions 16, 15 and gate electrode 18 of Koike et al (Figure 2) correspond to regions 2, 3 and gate electrode 6 of Nagasaki et al (Figures 3, 6) and to regions 26, 30 and gate 28 of acknowledged prior art Figure 1.

Claims 2, 8, 10, 20, 22, 23, 25, 34, 36, 37, 43, 47, 49, 50, 54, 60, 62 and 63 stand rejected under 35 USC 103 as unpatentable, the evidence being the acknowledged prior art in this application (Figures 1, 2 pages 1-12) and Nagasaki et al applied as in the above rejection, further considered with Suzuki. The claimed materials silicon nitride with silicon oxide (NO or ON) (claims 8, 10, 11, 20, 22, 23, 34, 36, 37, 47, 49, 50, 60, 62, 63), used by Suzuki (column 4) beneath photoelectrode 14, are well known to have a higher dielectric constant than silicon oxide, as applicant agrees (37 CFR 1.56, MPEP 2144.03), which would have been obvious to use for a photogate insulator in order to achieve a higher capacity for the photogate 24. Further, "polysilicon" (polycrystalline silicon) (claims 25, 43, 54) would have been obvious to use for a photogate 24, as in the acknowledged prior art Figure 1 similar to polysilicon photoelectrode 14 of Suzuki, in order to achieve a photogate electrode. Photoelectrode 14 of Suzuki (Figure 2) corresponds to transparent electrode 21 of Nagasaki et al (Figures 3, 6) and photogate 24 of acknowledged prior art Figure 1.

Claims 1-4, 7-15, 18-23, 25-29, 31-39, 41-63, 65, 115-125 and 135-149 stand rejected under 35 USC 103 as unpatentable, the evidence being the acknowledged prior art in this application (Figures 1, 2; pages 1-12) and Nagasaki et al, applied as in the above rejection, further considered together with Okada et al and Anagnostopoulos et al. The claimed material ONO (oxide-nitride-oxide) (claims 9, 13, 21, 35, 48, 52, 61, 65), used by Okada et al and Angnostopoulos et al, is well known to have a higher dielectric constant than silicon oxide as applicant agrees (37 CFR 1.56, MPEP 2144.03), which would have been obvious to use for a photogate insulator in order to achieve a higher capacity for the photogate. Note that an ONO layer comprises a "NO" layer and an "ON" layer (claims 8, 10, 11, 20, 22, 23, 34, 36, 37, 47, 49,

50, 60, 62, 63). Moreover, it would have been obvious to use a silicon nitride layer for (claims 7, 12, 19, 33, 38, 46, 51, 59) or within a photogate insulator (claims 1, 14, 28, 39, 53), because silicon nitride has a higher index of refraction which improves light transmittance through the gate electrode, and because silicon nitride blocks indium from leaching out of an indium tin oxide photogate and into the substrate (Anagnostopoulos et al, columns 3-4). Furthermore, it would have been obvious to use a silicon nitride layer to enhance reliability in terms of electric strength for or within a photogate insulator (Okada et al, column 12, lines 29-31). Furthermore, the claimed materials "polysilicon" and "indium tin oxide" (claims 2, 4, 25, 27, 43, 45, 54, 56) are conventional to use as transparent or semi-transparent materials, as shown by Anagnostopooulos et al (columns 1, 3-6), which would have been obvious to use to achieve a transparent or semi-transparent photogate electrode.

Claims 126-134 and 140-144 are rejected under 35 USC 103 as unpatentable, the evidence being acknowledged prior art in this application (Figures 1, 2, pages 1-12), Nagasaki et al, Okada et al and Anagnostopoulos et al, as in the above rejection further considered together with Koike et al, applied as in the above rejection of these claims.

The conclusion is that the claimed invention as a whole would have been obvious at the time the invention was made. The hypothetical person of ordinary skill in the relevant art, familiar with all that the acknowledged prior art, Nagasaki et al, Okada et al, Anagnostopoulos et al and Koike et al disclose, "would have found it obvious to make a structure corresponding to *what is claimed.*" *In re Sovish*, 226 USPQ at 774.

(10) Response to Argument

The Brief (pages 6-7) still fails to point out any language in claim 1 that distinguishes over Anagnostopoulos et al, because an insulating layer beneath an electrode 30 is perforce spatially distinct from an insulating layer beneath an electrode 32, even if those layers are subportions of a greater layer. Note for example that Alexandria is distinct from Arlington Country even if both are subportions of Virginia. Claim 1 does not specify how the "second" layer is distinct from the "first" layer apart from being beneath the "photogate" rather than beneath the "first and second gates stacks". Moreover, the Brief (pages 6-7) ignores Figure 3A, in which ONO layer 35, 34, 36 "beneath said photogate" 30 is clearly "distinct from said first insulating" layer 36 "beneath" electrodes 32. Contrary to the Brief (page 7), in present claim 9, the bottom layer of the ONO layer in contact with said substrate would be an oxide layer just like layer 43 of Anagnostopoulos et al.

Contrary to the Brief (page 12), the proper approach under 35 USC 103 is not what "would be acceptable to Nagasaki." Instead the proper approach is whether the hypothetical person of ordinary skill in the relevant art, familiar with all that the acknowledged prior art and Nagasaki et al disclose, "would have found it obvious to make a structure corresponding to *what is claimed*." *In re Sovish*, 226 USPQ at 774.

From Nagasaki et al (column 2, lines 22-24, column 3, table 1) silicon nitride and silicon oxide were conventional materials for use as a photogate insulator, and it would have been obvious to use conventional silicon nitride or conventional silicon oxide as a photogate insulator, and to use conventional silicon nitride in order to achieve a higher capacity of the photogate than the use of conventional silicon oxide. It also would have been obvious that the materials used in

this invention would achieve a lower capacity of the photogate than would use of tantalum oxide as in Nagasaki et al, because tantalum oxide has a higher dielectric constant than silicon nitride, while silicon nitride has a higher dielectric constant than silicon oxide. Thus, this invention appears to be in accordance with the teachings of Nagasaki et al. From Nagasaki et al, to increase the capacity of a photogate by use of an insulator with a higher dielectric constant, obviously silicon nitride remains more desirable than silicon oxide, even if tantalum oxide would have been more desirable than silicon nitride or silicon oxide.

Moreover, the Brief (pages 9-10, 12, 18) ignores Figures 3 and 6 of Nagasaki et al. Contrary to the Brief (pages 12, 18), Figures 3 and 6 show a transparent photogate electrode 21. Contrary to the Brief (page 9), Nagasaki et al (Figure 6) show insulating film 4 beneath photo-gate electrode 21 while silicon dioxide insulating film 22 is beneath gate electrode 6.

Contrary to the Brief (page 18), Okada et al and Anagnostospoulos et al would have provided motivation to use silicon nitride for, or with, an insulating layer beneath photogate 24 of acknowledged prior art Figure 1. It would have been obvious to use a silicon nitride layer for a photogate insulator, because silicon nitride has a higher index of refraction which improves light transmittance through the gate electrode, and because silicon nitride blocks indium from leaching out of an indium tin oxide photo gate and into the substrate (Anagnostopoulos et al, columns 3-4). Furthermore, it would have been obvious to use a silicon nitride layer to enhance reliability in terms of dielectric strength for a photogate insulator (Okada et al, column 12, lines 29-31).

Contrary to the Brief (page 17), Suzuki (Figure 2, column 4) does teach use of silicon nitride with silicon oxide (NO or ON) beneath a photoelectrode 14. The present claimed "photogate" corresponds to photoelectrode 14 of Suzuki (Figure 2), transparent electrode 21 of Nagasaki et al (Figures 3, 6) and photogate 24 of acknowledged prior art Figure 1.

Contrary to the Brief (page 15), Koike et al (columns 3-4) do teach the use of "polysilicon" (polycrystalline silicon), "tin oxide" (SnO_2) and "indium oxide" (InO_2) for a transparent or semi-transparent electrode. Koike et al (Figure 2) also teach the "photogate" insulator 21 and electrode 22 disposed at least in part over the adjacent gate electrode 18. Note that appellant "cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references." *In re Keller*, 208 USPQ 871, 882 (CCPA 1981).

It is submitted that the claims are properly rejected as unpatentable, as explained above.

Respectfully submitted,

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